DOCUMENT-IDENTIFIER: JP 10223772 A
TITLE: CMOS SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

FPAR:
PROBLEM TO BE SOLVED: To provide a method of forming an NMOS and a PMOS into an LLD structure and a single drain structure respectively, wherein source-drain regions of PMOS are not required to be formed excessively deep.

FPAR:
SOLUTION: A gate electrode 5 is formed on an N-type well region 3 and a P-type well region (not shown) though the intermediary of a gate insulating film 4 (a). As<SP>+</SP> 6 is implanted for the formation of an N-type low-concentration region 7 (b). A side wall spacer 8 is formed on the side of the gate electrode 5 (c). A resist film is formed on the N-type well region 3, and the P-type well region (not shown) is doped with N-type impurities high in concentration for the formation of source-drain regions of LDD structure (d). The surface of the side wall spacer on a PMOS forming region side is lessened in width by etching (e). BF<SP>+</SP> 10 is injected to from P<SP>+</SP>-type source-drain regions 11 (f).

CLIPPEDIMAGE= US005254866A
PUB-NO: US005254866A
DOCUMENT-IDENTIFIER: US 5254866 A
TITLE: LDD CMOS with wider oxide sidewall on PMOS than NMOS

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PRIORITY-DATA: JP08950890A (April 3, 1990)
INT-CL_(IPC): H01L027/092
EUR-CL (EPC): H01L021/336; H01L021/336, H01L021/8238 , H01L027/092

ABSTRACT:
A semiconductor device comprises a semiconductor substrate (11) having first and second field effect transistors. Each transistor includes a gate electrode (17, 18) formed on the semiconductor substrate with a gate insulating film (15, 16) interposed therebetween. A first side wall spacer (21, 22) formed of one layer of an insulating film on opposite side wall surface of the gate electrode, and source/drain regions (19, 24, 26, 30), each comprising high and/or low impurity concentration regions of the gate electrode (17, 18) on the surface of the semiconductor substrate (11). A second side wall spacer (27, 28) formed of another layer of an insulating film formed at least one side wall surface of the gate electrode (17, 18) of at least said second transistor. The first and/or the second side wall spacers (21, 22, 27, 28) form diffusion masks for adjusting distribution of impurity concentration of the transistors. Due to this structure, the widths of the side wall spacers (21, 22, 27, 28) as diffusion masks which are responsive to required characteristics, are attained for respective side walls of the gate electrodes (17, 18). The semiconductor device of such structure is manufactured by implanting impurity ions between the steps of forming the first and the second side wall spacers (21, 22, 27, 28) and each time covering prescribed region with a resist film (20, 23, 25, 29, 31, 33, 35).

DOCUMENT-IDENTIFIER: JP 63246865 A
TITLE: CMOS SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

TTL:
CMOS SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

FPAR:
PURPOSE: To obtain excellent balance in electric characteristics, by making the width of a side wall for a gate electrode provided in a PMOS semiconductor element narrower than the width of a side wall provided in an NMOS semiconductor element.

FPAR:
CONSTITUTION: A side wall 31b is arranged in an NMOS semiconductor element 49 having an LDD (Lightly Doped Drain) structure. A side wall 55, whose width is narrower than the side wall 31b, which is provided in the NMOS semiconductor element 49, is provided in a PMOS semiconductor element 59. Thus a CMOS semiconductor device 61 is completed. In this way, hot carriers in the NMOS semiconductor element 49 are prevented, and the CMOS semiconductor element, in which parasitic resistance and parasitic capacitance are balanced on the side of the PMOS semiconductor element 59, is obtained.

DOCUMENT-IDENTIFIER: JP 2000232166 A
TITLE: MANUFACTURE OF SEMICONDUCTOR DEVICE

FPAR:
PROBLEM TO BE SOLVED: To provide a semiconductor device manufacturing method by which the short-channel effect of a CMOS transistor can be suppressed and the current driving ability of the transistor can be improved, and then, the density of the transistor can be increased.

FPAR:
SOLUTION: A semiconductor device manufacturing method includes a step for selectively introducing an n-type impurity to an nMOS transistor forming area 1 by using a gate electrode 5 as a make, a step for forming first side walls 7 on the side faces of gate electrodes 5, and a step for selectively introducing a p-type impurity to a pMOS transistor forming area 2 by using another gate electrode 5 and first side walls 7 formed on the side faces of the electrode 5 as masks. The method also includes a step for forming second side walls 9 which are narrower in width than the first side walls 7 on the side faces of the electrodes 5 after removing the first side walls 7, and a step for selectively introducing the n- and p-type impurities to the nMOS and pMOS transistor forming areas 1 and 2, respectively, by using the gate electrodes 5 and second side walls 9 as masks.

L Number	Hits	Search Text	DB	Time stamp
1	6	CMOS and PMOS and NMOS and ((side with walls) same width)	EPO; JPO; DERWENT; IBM TDB	2002/03/19 14:00
2	101	CMOS and PMOS and NMOS and ((side with walls) same width)	USPAT; US-PGPUB	2002/03/19 14:01
3	141	PMOS and NMOS and ((side with walls) same width)	USPAT; US-PGPUB	2002/03/19 14:02
4	0	(CMOS and PMOS and NMOS and ((side with walls) same width)) not (PMOS and NMOS and ((side with walls) same width))	USPAT; US-PGPUB	2002/03/19 14:02

DOCUMENT-IDENTIFIER: US 5994743 A
TITLE: Semiconductor device having different sidewall widths and different source/drain depths for NMOS & PMOS structures

ABPL:
A CMOS device includes a first conductive type channel MOSFET having first side-wall spacers on side surfaces and having a source and drain region of an LDD structure, and a second conductive type channel MOSFET having second side-wall spacers on side surfaces and having a source and drain region of a single drain structure, wherein a width of the first side-wall spacers is larger than that of the second side-wall spacers, restraining the short channel effect and hot carrier effect as well.

BSPR:
The present invention relates to a complementary metal oxide semiconductor (hereinafter, referred to as CMOS) device having an n-channel and a p-channel metal oxide semiconductor field effect transistors (or n-channel and p-channel MOSFETs) and manufacturing method of the same, more particularly to a CMOS device and manufacturing method thereof capable of restraining short channel effect of the n-channel and p-channel MOSFETs without increasing the number of photolithography processes.

BSPR:
In addition, other CMOS devices and manufacturing methods have proposed such that an nMOSFET should only be made into the LDD structure while both an nMOSFET and a pMOSFET should be made into the LDD structure.

BSPR:
That is, The document of Japanese Laid-Open Patent Application No. Hei3-41763 discloses the following process: a gate electrode is formed on an nMOSFET forming region and a pMOSFET forming region and n.sup.- -type region is formed in the nMOSFET forming region with a resist film coated on the pMOSFET forming region; side-wall spacers are formed on the side surfaces of gate electrode for the nMOSFET and an n-type impurity is doped into the nMOSFET forming region in high concentration to form an n.sup.+ -type region with a resist film coated on the pMOSFET forming region; and other side-wall spacers, width of which is wider than that of nMOSFET, are formed on the side surfaces of gate electrode of the pMOSFET forming region and a p-type impurity is doped into the pMOSFET forming region in high concentration to form a p.sup.+ -type source and drain region with a resist film coated on the nMOSFET forming region.

source and drain region 115. Therefore, since the n-type low concentration region 109 should remain to a certain extent in the nMOSFET forming region, it is desirable that the side-wall spacers 111, which become masks in the ion-implantation of As.sup.+ shown in FIG. 3(f), are formed thick in consideration of the width in a lateral direction of the n-type high concentration region 119. However, since the pMOSFET side is used by the process to be inverted by the ion-implantation of B.sup.+ as shown in FIG. 3(e) after forming a conductive type of the n-type low concentration region as side-wall spacers, the p-type high concentration source and drain region should be formed to some extent of depth in case of forming the side-wall spacers in thick. To this end, the junction depth of the p-type high concentration source and drain region in the pMOSFET region becomes deeper than that of the n-type high concentration source and drain region in the nMOSFET region. As a result, the short channel effect of the pMOSFET becomes remarkable, so that the critical dimension of the gate length for the pMOSFET is limited.

BSPR:
According to a first aspect of the present invention, there is provided a CMOS device including: a first conductive type channel MOSFET having first side-wall spacers on side surfaces thereof and having a source and drain region of an LDD structure; and a second conductive type channel MOSFET having second side-wall spacers on side surfaces thereof and having a source and drain region of a single drain structure, in which a width of the first side-wall spacers is larger than that of the second side-wall spacers.

BSPR:
According to a second aspect of the present invention, there is provided a method of manufacturing the CMOS device including the steps of: (1) forming first and second gate electrodes on first and second conductive type semiconductor regions through a gate insulation film, respectively; (2) doping a first conductive impurity into the first and second conductive type semiconductor regions in low concentration with use of the first and second gate electrodes as mask to form a first conductive type low concentration region within surface areas of the first and second conductive type semiconductor regions at both sides of the first and second gate electrodes; (3) forming an insulation film entirely and carrying out an etch back to form first and second side-wall spacers on side surfaces of the first and second gate electrodes, respectively; (4) laminating the first conductive type semiconductor region by a first mask and doping a first conductive type impurity thereinto in high concentration with use of the first mask, the first gate electrode and the first side-wall spacers as mask to form a first conductive type high concentration region within the surface area of the second conductive type semiconductor region at outside of the first side-wall spacers; and (5) applying an isotropic etching treatment

step (4) and step (5).

BSPR:
In the process of manufacturing a CMOS device for forming nMOSFET of the LDD structure and pMOSFET of the single drain structure, since the ion-implantation is carried out to form the p-type source and drain region after forming the side-wall spacers of the pMOSFET, width of which is smaller than those of the nMOSFET, the conductive type of n-type low concentration region (LDD structure) can be inverted even if the source and drain region of pMOSFET may be relatively shallow. Thus, the junction depth of the source and drain region in pMOSFET can be made shallow or equal to that of the source and drain region in nMOSFET, restraining the short channel effect of pMOSFET to achieve a fine or critical dimension of device. Furthermore, the LDD structure (or n-type low concentration region) in the nMOSFET is sufficiently secured, restraining the short channel effect and hot carrier effect as well.

DRPR:
FIGS. 1(a) to 1(f) are sectional views showing a manufacturing process of a CMOS device in an embodiment of the present invention;

DRPR:
FIGS. 2(a) to 2(g) are sectional views showing a manufacturing process of a CMOS device in another embodiment of the present invention; and

DRPR:
FIGS. 3(a) to 3(f) are sectional views showing a manufacturing process of a CMOS device for explaining a related art.

DEPR:
FIGS. 1(a) to 1(f) are sectional views showing the order of a manufacturing process of a CMOS device in an embodiment of the present invention.

DEPR:
According to the manufacturing method described above, when forming the p.sup.+ -type source and drain region 11 in the case of pMOSFET, the width of side-wall spacers 8, 8 are made small, as shown in FIG. 1(f), therefore, the conductive type of n-type low concentration region 7 can be inverted without ion-implanting a p-type impurity thereon and making it deep. Thus, the junction depth of p.sup.+ -type source and drain region 11 can be made shallow, restraining the short channel effect. While in the case of nMOSFET, the width of side-wall spacers are made sufficiently larger to eventually form a desirable length of the n-type low concentration region 7 as an LDD structure region, restraining the short channel effect and hot-carrier effect as well.

1.5.times.10.sup.13 cm.sup.-2 in dose. The p-type well region 24 may also be formed by ion-implanting B.sup.+ thereon under conditions of 30 KeV in energy and 6.times.10.sup.12 cm.sup.-2 in dose, for example, after ion-implanting such B.sup.+ under conditions of 300 KeV in energy and 2.times.10.sup.13 cm.sup.-2 in dose. Subsequently, after forming a gate oxidation film 25 as much as 6 nm thick by the thermal oxidation method, a non-doped polysilicon is deposited thereon as much as 200 nm thick by the CVD method. Both a gate electrode 26 of nMOSFET and a gate electrode 27 of pMOSFET are then formed by the photolithography process and etching process.

CLPR:
1. A CMOS device including a first conductive type channel MOSFET having first side-wall spacers on side surfaces and having a source and drain region of an LDD structure; and a second conductive type channel MOSFET having second side-wall spacers on side surfaces and having a source and drain region of a single drain structure, wherein:

CLPR:
2. A CMOS device according to claim 1, wherein the first conductive type channel MOSFET has a gate electrode, the side surfaces of which have the first side-wall spacers, respectively.

CLPR:
3. A CMOS device according to claim 1, wherein the second conductive type channel MOSFET has a gate electrode, the side surfaces of which have the second side-wall spacers, respectively.

CLPR:
4. A CMOS device comprising:

CLPR:
5. A CMOS device according to claim 4, wherein the side-wall spacers are layers composed of SiO.sub.2.

CLPV:
a width of the first side-wall spacers is larger than that of the second side-wall spacers, and

CLPV:
wherein a width of the first side-wall spacers is larger than that of the second side-wall spacers; and a junction depth of the source and drain region in the first conductive type channel MOSFET is larger than that of the source and drain region in the second conductive type channel MOSFET.